Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-2. (Canceled)

3. (Currently Amended) ~~The microprocessor according to claim 2~~A microprocessor comprising:

a memory array having a stack for saving contextual data; and

a central processing unit coupled to the memory array, the central processing unit having registers containing contextual data and a stack pointer and being arranged for saving contextual data upon a switch from a first to a second program in a variable number of registers that varies according to a value of at least one flag stored in a register to be saved,

wherein the central processing unit is arranged for changing the value of the at least one flag according to the content of an extended addressing register of a program counter of the central processing unit before saving contextual data contained in a variable number of registers that varies according to the value of the at least one flag.

4. (Original) The microprocessor according to claim 3 wherein the central processing unit is arranged for:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; and

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

5. (Currently Amended) The microprocessor according to claim ~~1~~ 3 wherein the central processing unit is arranged for performing a test on the value of the at least one flag so as to determine the number of registers to be saved.

6. (Currently Amended) The microprocessor according to claim ~~1~~ 3 wherein the central processing unit is arranged for, upon the return to the first program:

restoring the register containing the at least one flag at a first time; and

restoring contextual data contained in a variable number of registers that varies according to the value of the at least one flag present in the restored register at a second time subsequent to the first time.

7. (Currently Amended) The microprocessor according to claim ~~1~~ 3 wherein the central processing unit is arranged for saving the register containing the at least one flag last.

8. (Currently Amended) The microprocessor according to claim ~~1~~ 3 wherein the at least one flag comprises at least one bit of a register containing condition code flags.

9-10. (Canceled)

11. (Currently Amended) ~~The method according to claim 10 wherein the value of the flag is changed according to the content of~~ A method for managing a stack of a microprocessor having a central processing unit and a memory array, the central processing unit having registers containing contextual data and a stack pointer, the stack being a zone of the memory array dedicated to saving contextual data upon a switch from a first to a second program, the method comprising:

saving contextual data contained in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved; and

changing the value of the at least one flag according to the content of an extended addressing register of a program counter of the central processing unit before saving the contextual data.

12. (Currently Amended) The method according to claim 11, comprising the following steps:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; ~~or~~and

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

13. (Currently Amended) The method according to claim ~~9~~11, comprising a step of:

testing the value of the at least one flag for determining the number of registers containing the data to be saved.

14. (Currently Amended) The method according to claim ~~9~~11, comprising the following steps:

restoring the register containing the at least one flag; then

restoring contextual data contained in ~~a~~the variable number of registers that varies according to the value of the at least one flag present in the restored register.

15. (Currently Amended) The method according to one claim ~~9~~11 wherein the register containing the at least one flag is saved last and is restored first.

16. (Currently Amended) The method according to claim ~~9~~11 wherein the at least one flag is formed by at least one bit of a register containing condition code flags.

17. (Currently Amended) A microprocessor comprising:

a memory array having stored therein contextual data;

a central processing unit coupled to the memory array;

a plurality of registers associated with the central processing unit, a first group of the registers storing contextual data and a second group of the registers not storing contextual data when a flag has a first value and switching to store contextual data also in the second group of registers when the flag switches to a second value, such that the number of registers that store contextual data is variable

and where the flag is stored in a register to be saved as part of the program contextual data and where the flag is asserted when an extended portion of a program counter has a portion of an extended address;

a stack pointer associated with the central processing unit and being arranged for directing contextual data to be stored in the first group only or in both the second group and the first group, based on the flag value.

18. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a register which is used as an extended addressing register when the flag is at a first value.

19. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a single register.

20-24. (Canceled)

25. (New) A microprocessor based system comprising:

a memory array;

a first amount of contextual data stored in at least one register, the register having at least one flag;

a central processing unit coupled to the memory array and operable upon a program switch to save the first amount of the contextual data and, if the flag is asserted, a second amount of the contextual data, wherein the central processing unit is further operable upon a return from a program switch to restore the first amount of contextual data and, if the flag is asserted, to subsequently restore the second amount of contextual data.

26. (New) The microprocessor based system according to claim 25 further comprising a program counter, wherein the flag is asserted when an extended portion of the program counter contains an extended address value.

27. (New) The microprocessor based system according to claim 25 further comprising a program counter, wherein the flag is not asserted when an extended portion of the program counter contains a null address.

28. (New) A method of handling contextual data during program switch operations comprising:

asserting a flag if an extended portion of a program counter is not null;

copying into a memory during a program switch, a first amount of contextual data including the flag and, if the flag is asserted, copying a second amount of contextual data; and

restoring the first amount of contextual data during a return from the program switch and, if the flag is asserted, restoring the second amount of contextual data.

29. (New) The method according to claim 28 wherein the flag is asserted when the extended portion of the program counter contains an extended address value.

30. (New) The method according to claim 28 further comprising updating a stack pointer by a first amount if when a first amount of contextual data is copied and updating the stack pointer by a second amount if the second amount of contextual data is copied.